System Power Integrity Analysis: PMIC to Transistor

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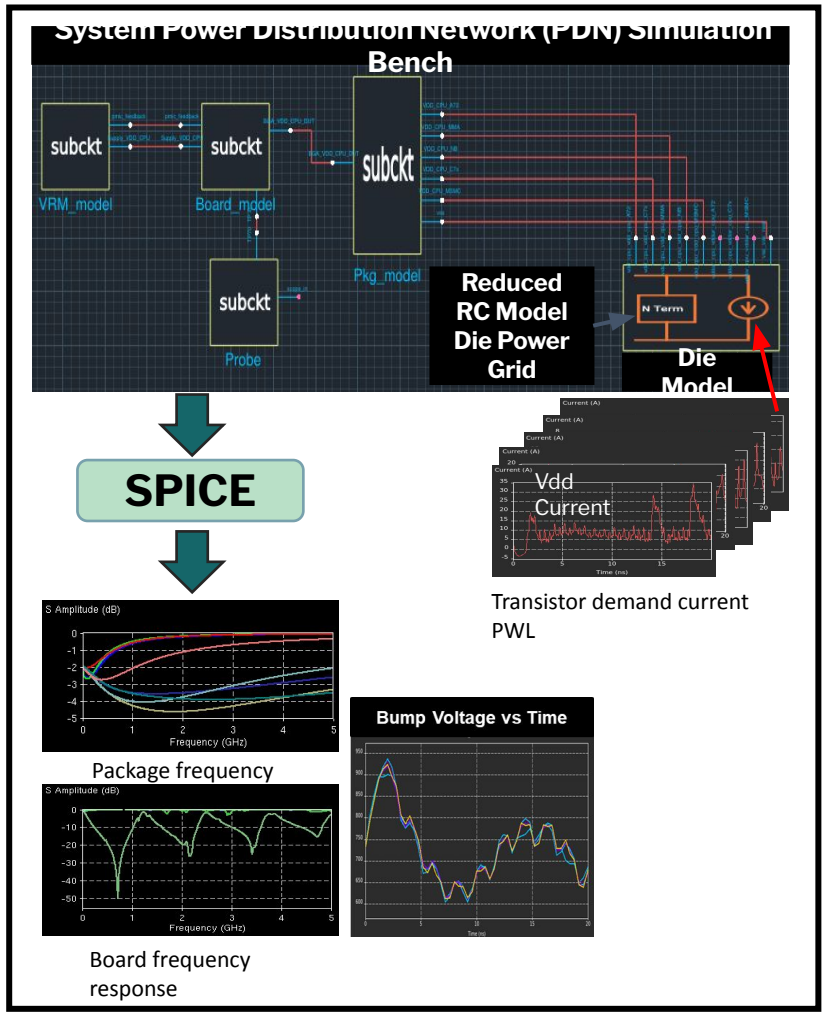
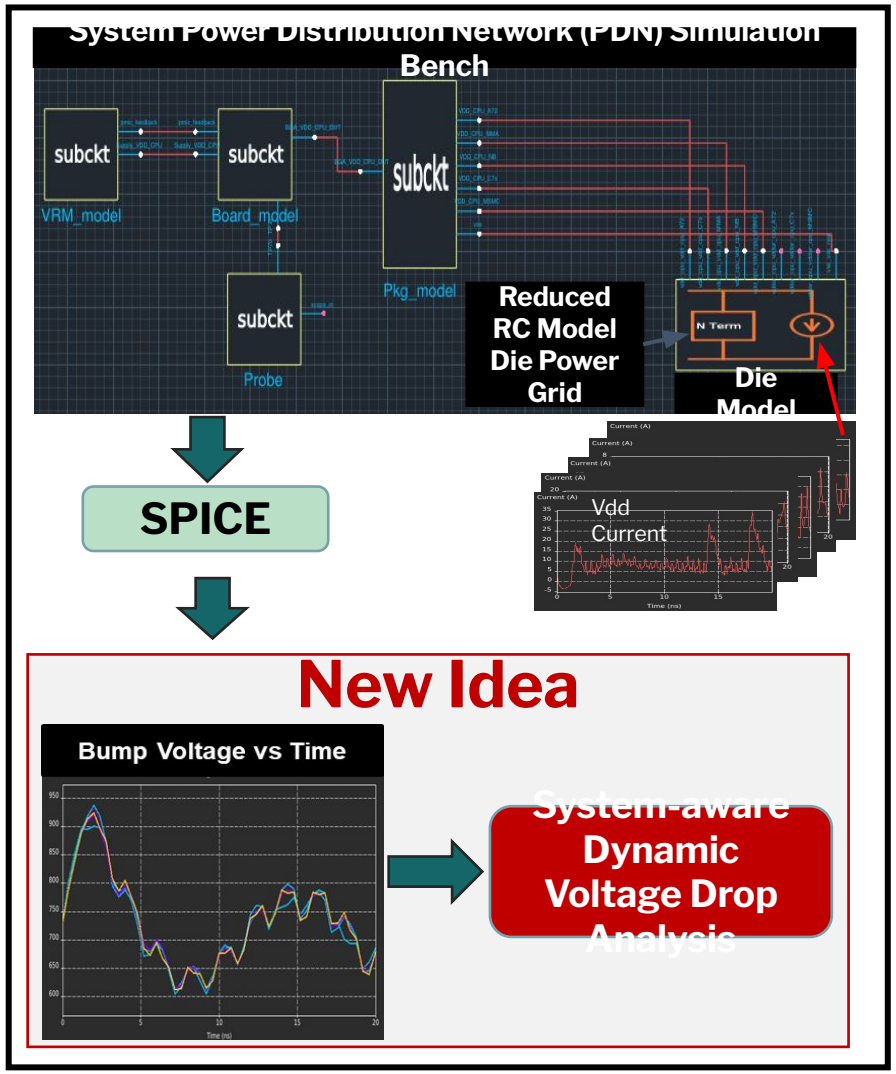
Motivation

- Goal: IR drop analysis including voltage variation of System Power Distribution Network (PDN).
  - Traditionally, SoC die-only IR drop signoff analysis is performed using ideal supply voltages at the die power ground (PG) pins.
  - Co-simulation of die, package, board and voltage regulator module (VRM) challenges EDA tool capacity and accuracy.
- Common workarounds include divide-and-conquer using discrete die-only and system PDN simulations.
  - These typically result in accuracy tradeoffs, especially when estimation to transistor and other on-die devices is needed.
  - Lack of co-simulation increases the likelihood of overly conservative design margin or costly design revisions.



Requirements

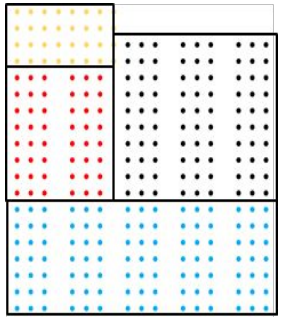
- A novel methodology for detailed analysis of on-die IR drop including System PDN voltage variation.
  - Accurate board, package and die co-simulation of dynamic voltage delivery to the SoC transistors.
- Solution must address common IC Signoff Dynamic IR drop analysis tool limitations:
  - Turn-around-time (TAT) and capacity challenges introduced by very large SoC-level vectors and System PDN electrical models.
  - Consume S-parameter models for package and board.
- New idea:
  - IC signoff tools import a SPICE-accurate PWL model of bump voltage.
  - Utilize time-variant bump voltage model to assess the impact from System PDN in dynamic IR drop analysis.



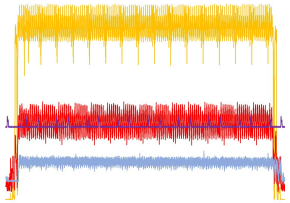
New Methodology

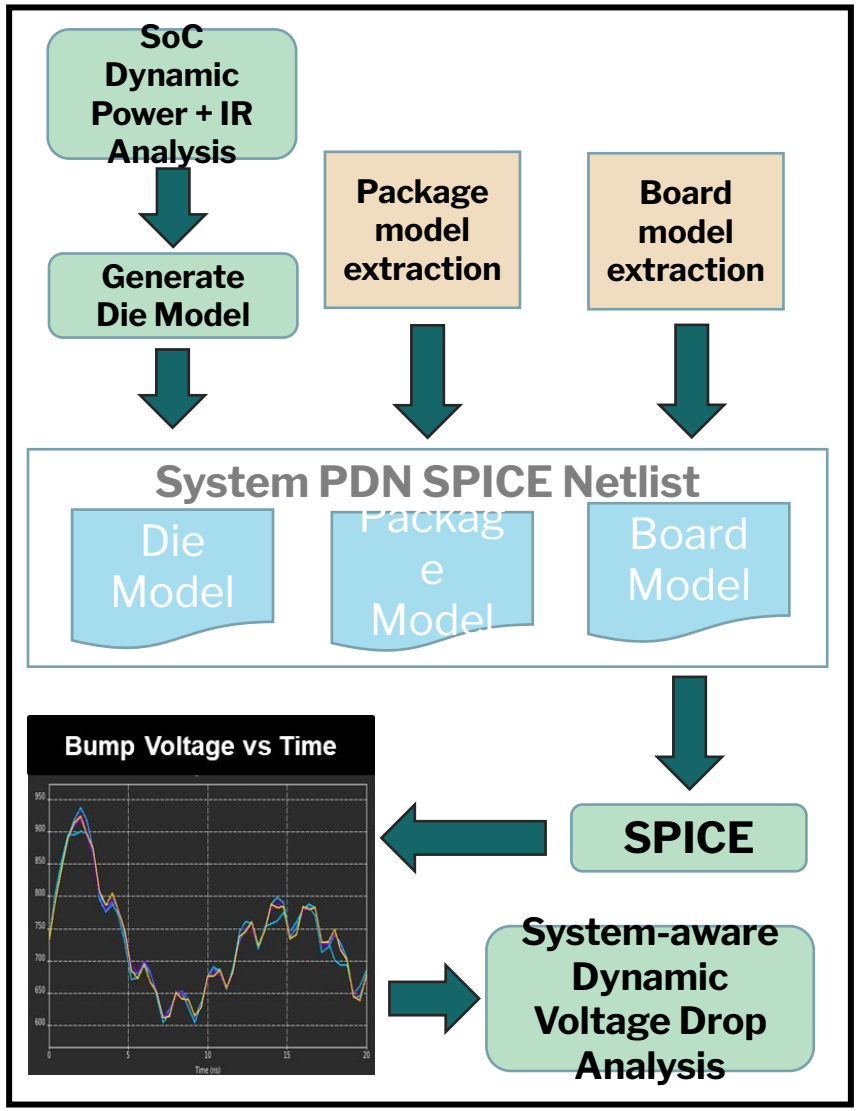
- Standard practices:
  - SoC Die Model includes:
    - Reduced RC network of extracted on-die power grid.
    - Transistor demand current profile
      - Piece-wise linear (PWL) models.
      - **New** : Bump groups by block boundary.
  - Extract package S-parameter model.
  - Extract board S-parameter model.
  - SPICE simulation of System PDN.
- Proposed solution uses those results:
  - Extract PWL model of bump voltage.
  - Vector-based Dynamic IR analysis with bump voltage model.

Bump Groups by Block Boundary



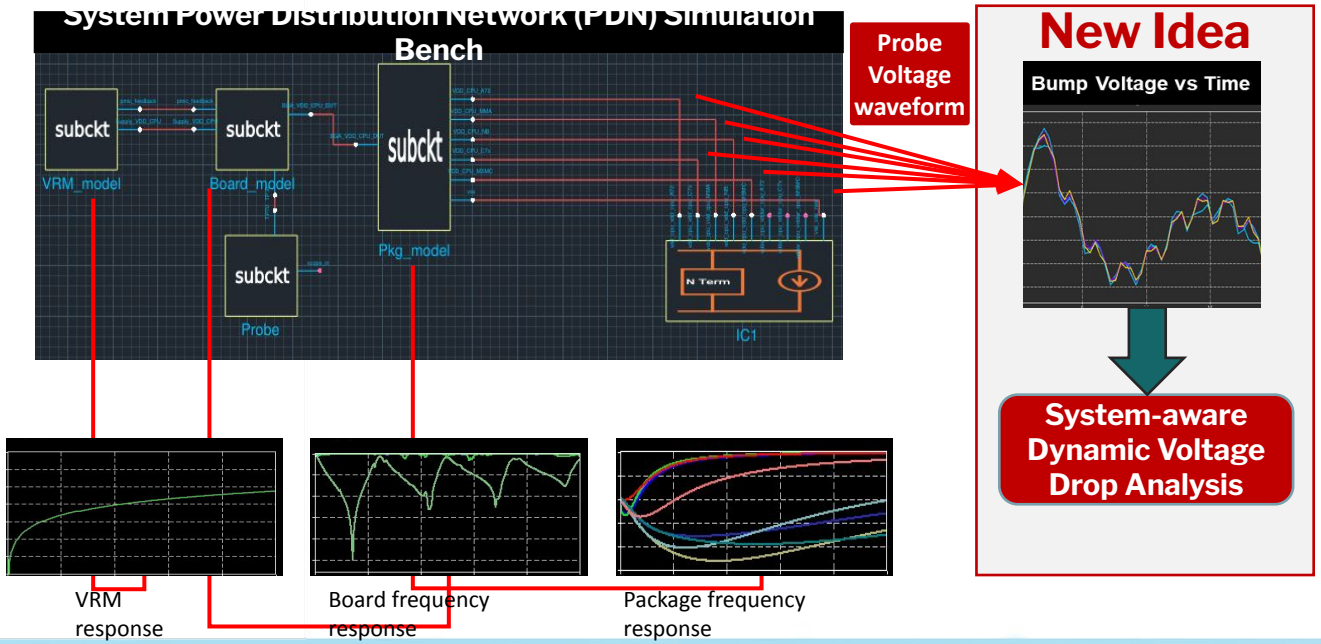
Current profiles by Block Boundary



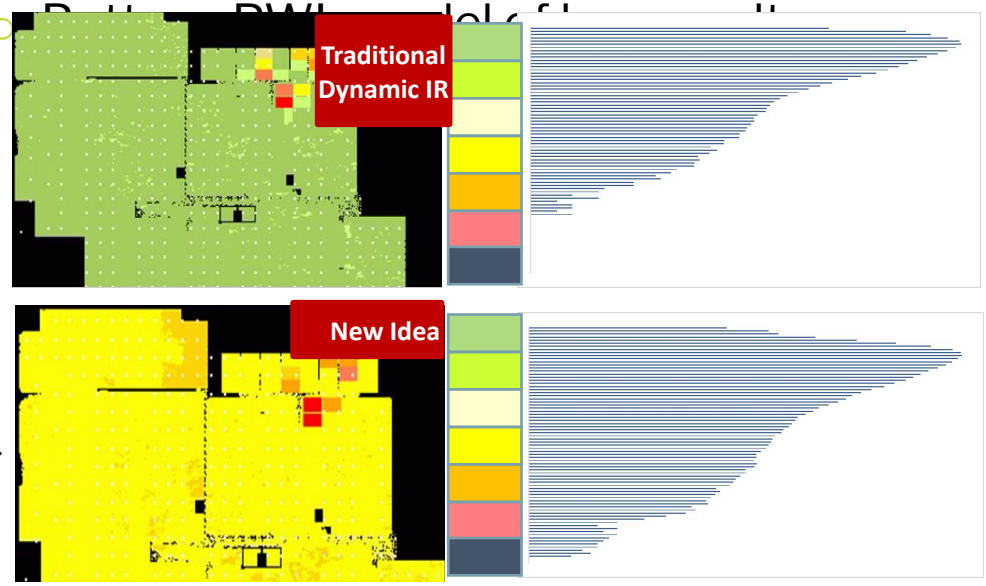


Results

- Step #1:
  - System PDN Analysis:
    - Die model created and connected to electrical package & board models.
    - SPICE simulation of System PDN.
    - Capture die bump voltage PWL model.

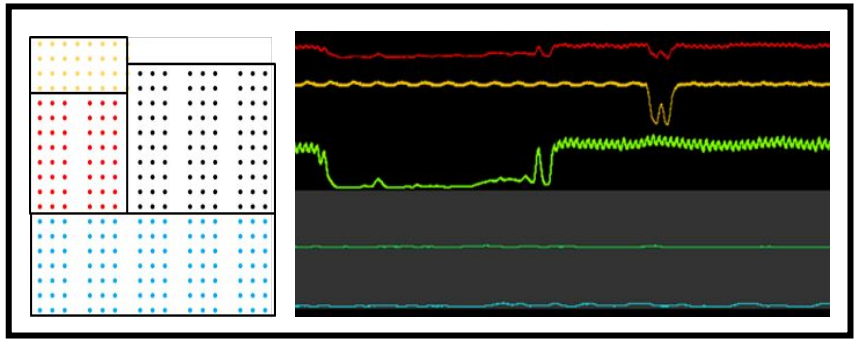


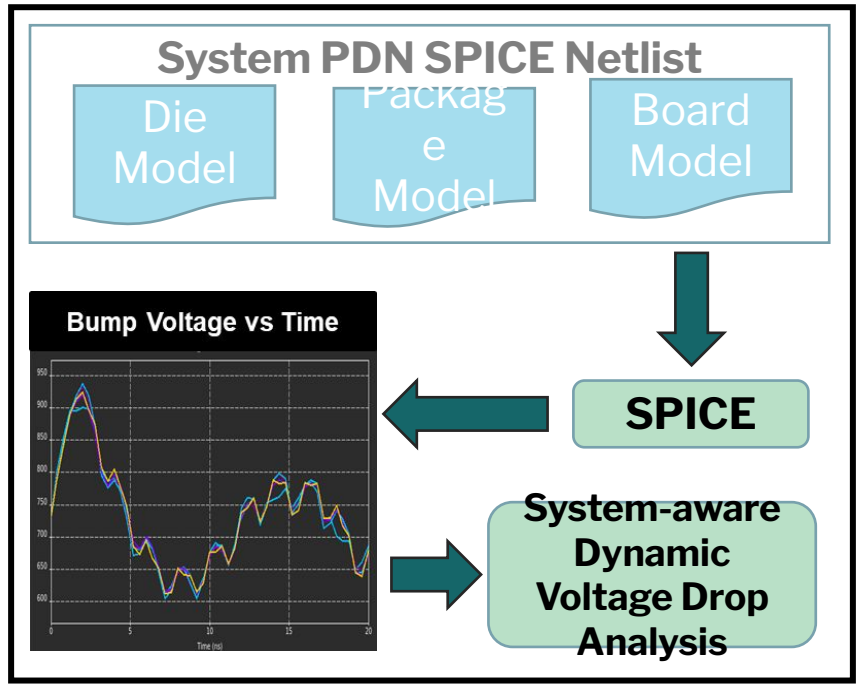
- Step #2:
  - Execute new PDN-aware die IR analysis and confirm that Vdd-Vss differential voltage drop vs. reference increases no more than 5% :
    - Top: with traditional DC bump model.



Attainment

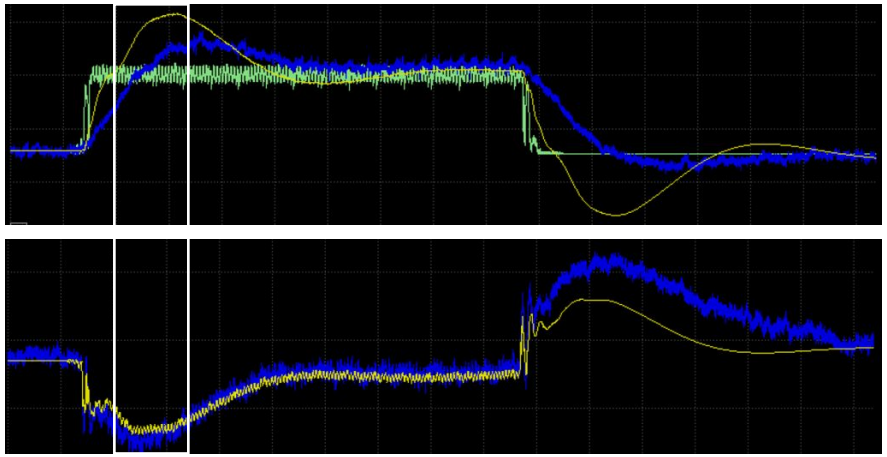
- Proposed solution meets IC signoff tool requirements :
  - Die models for System PDN analysis utilize power profiling.
    - System time constants do not require full IR flow resolution.
    - Utilizing an appropriate resolution significantly improves the TAT and capacity in the analysis of very large SoC-level vectors.
  - Use of SPICE-accurate PWL model of bump voltages greatly improves the TAT and capacity of these analyses.
    - System PDN analysis already consumes more accurate S-parameter models, eliminating limitations with simple SPICE models.
    - System PDN analysis already consumes board models, and therefore are accurately modeling a complete System PDN filter network.

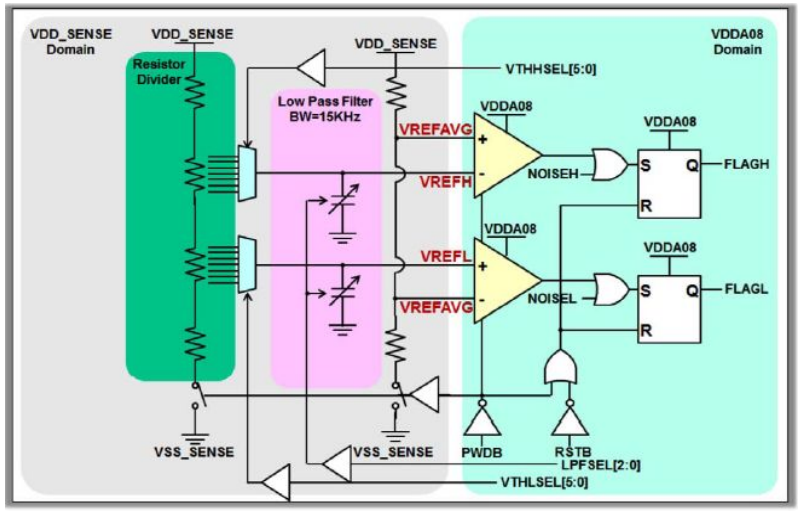




Future Work

- Silicon correlation :
  - Incorporate demand challenging current profiles into PDN-aware Dynamic IR analysis.
  - Use on-die Power Glitch Detector (PGD) to correlate simulated die bump voltage versus bench data.
    - IEEE SPI 2023 “Techniques for Correlating Power Distribution Network Simulations with Physical Measurements” (Cano, et al).
    - Simple operation: set threshold, run test, check if threshold was triggered.
    - Area efficient, single supply, 400MHz bandwidth.
    - However, no waveform capture and synchronization to application code is challenging.



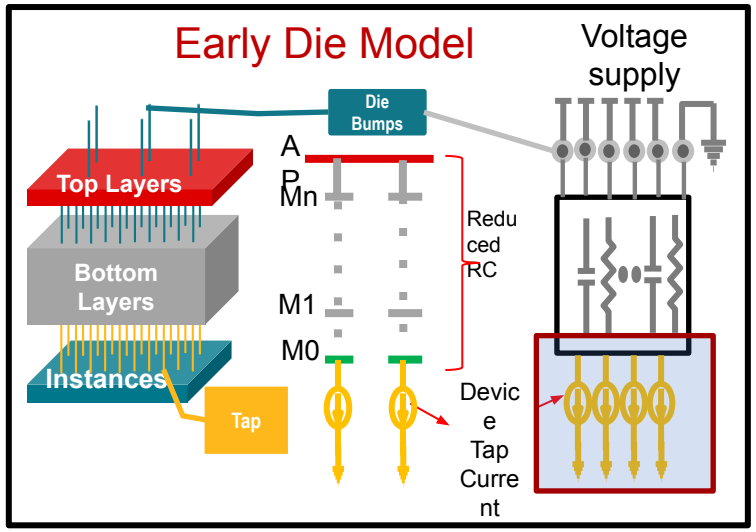


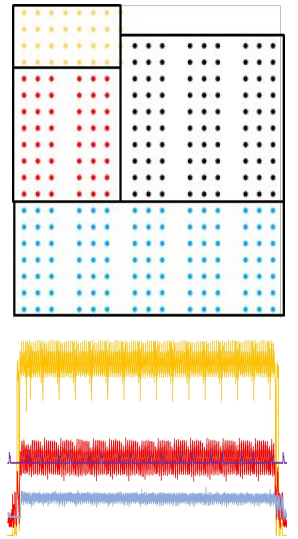
[R. Venkatasubramanian 2020] "2.6 A 16nm 3.5B+ Transistor >14TOPS 2-to-10W Multicore SoC Platform for Automotive and Embedded Applications with Integrated Safety MCU, 512b Vector VLIW DSP, Embedded Vision and Imaging Acceleration,"

Continuous Improvement

Bump Groups by Block Boundary

- PDN co-simulation flow continuous improvement:
  - Early analysis method needed prior to silicon tape-out or package and board design lock.
  - Die models use bump groups based on block boundaries to enable more plug-n-play demand current models.
  - Use results to drive subchip IR drop signoff analysis with PWL model of bump voltage.
  - Continuously improve both model and analysis quality.
- Silicon correlation :
  - Convergence of transistor demand current in the context of time-variant bump supply voltage.
  - Need on-chip oscilloscope to correlate waveforms.





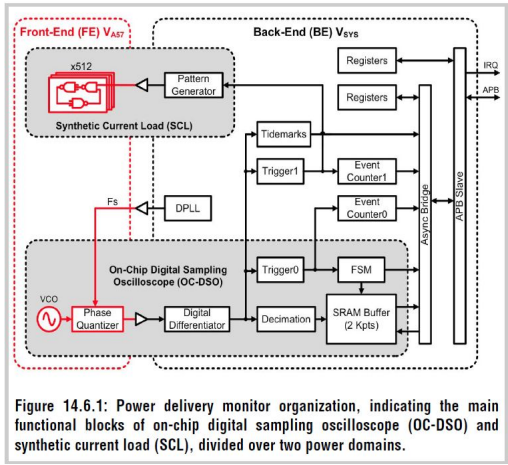


Figure 14.6.1: Power delivery monitor organization, indicating the main functional blocks of on-chip digital sampling oscilloscope (OC-DSO) and synthetic current load (SCL), divided over two power domains.

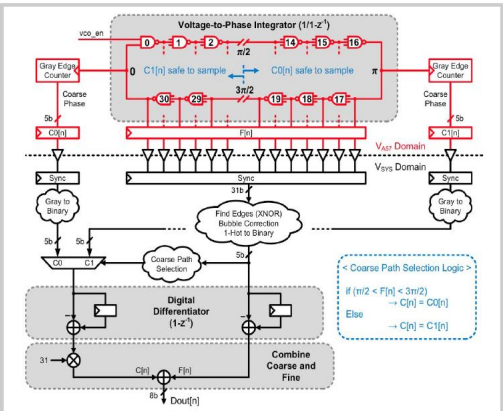


Figure 14.6.2: All-digital A/D conversion by sampling a free-running VCO with two coarse stages and a fine stage.

[Whatmough 2015] "On chip digital oscilloscope and synthetic current load"

Summary

- SoC IR drop signoff utilizing full System PDN voltage variation.
  - New method greatly improves accuracy of estimation to transistor.
  - Power-Performance-Area (PPA) improvements from reduced design margins and minimum SoC supply voltage.
- Demonstrates accurate analysis using PDN voltage variation.
  - Less conservative relative to traditional superposition of die-only IR result with System PDN peak-to-peak noise.
  - Dynamic IR with system-accurate bump voltages shows significant impact versus constant DC supply voltages.
- Efficient SoC and System analysis tool interface.
  - Solution closes electrical and physical loop from PMIC to transistor.
  - Improves confidence of the on-die Dynamic IR signoff.